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TITLE: Dynamic rate control technique for video multiplexer

Abstract Text (1):
A video multiplexer is disclosed which incorporates a dynamic rate control feature. MPEG encoded video signals for each channel are stored in a first-in first-out (FIFO) buffer. A packetizer for each channel detects the level in the FIFO buffer and issues a request signal to the video multiplexer that the channel desires to transmit the video signals on the network. The bandwidth allocation for a channel is either preselected by the video provider or automatically selected, and tokens are issued by a counter associated with each channel to give greater network access to those channels which require a higher bandwidth. A token multiplier detects the bandwidth needs of the various channels by detecting the rate that the FIFO buffer is being filled and automatically multiplies the number of consecutive packets which the packetizer may transmit over the multiplexer during a single grant.

Application Filing Date (1):
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Brief Summary Text (2):
This invention relates to video multiplexers and, in particular, to a technique for allocating bandwidths to video channels connected to the multiplexer.

Brief Summary Text (11):
In the preferred embodiment, the bandwidth allocation for a channel is either preselected by the video provider or automatically selected, and tokens are issued by a counter associated with each channel to give greater network access to those channels which require a higher bandwidth. A variable token bucket for each channel stores the issued tokens until needed. A token multiplier detects the bandwidth needs of the various channels by detecting the rates that the FIFO buffers are being filled and automatically multiplies the number of accumulated tokens for the

Detailed Description Text (18):
Issuing requests for grant rather than waiting for the multiplexer 50 (or arbiter) to poll the packetizers results in a time savings and memory savings in that the packetizers 44 do not have to wait to be polled before being issued access to bus 52. Thus, channels which are not generating data or which are generating data very slowly do not delay bus access to a packetizer which needs access to bus 52. The structure shown in FIG. 1 is also very economical as compared to prior art video processors in that the packetizing is performed by each channel prior to being multiplexed. In certain prior art structures, an ATM switch receives the raw MPEG data, multiplexes the data and packetizes the data. Such a prior art ATM switch is more expensive than the multiplexing circuitry shown in FIG. 1 since multiplexer 50 does not have to be synchronized with the MPEG data in the various channels and thus results in a simpler system. Additionally, the system of FIG. 1 allows for customized or automatic bandwidth allocation to the various channels as described below.

Detailed Description Text (22):
To allocate different bandwidths to each channel at any time, a controller, using

an external personal computer 58, selects the bandwidths for each of the channels. This bandwidth allocation is performed using the functional blocks shown in FIG. 2.

Detailed Description Text (23):
Multiplexer 50 contains a counter 62 for each channel. In a preferred embodiment, counters 62 are 12-bit counters. If all channels were to be given an equal bandwidth allocation, then all counters 62 would be programmed by computer 58 to have the same modulus. A channel which is to be given a higher bandwidth allocation is programmed to have a lower modulus than the counters associated with channels with a lower bandwidth allocation. Once the counters are initially programmed, a register stores this program until changed by the external computer 58.

Detailed Description Text (25):
A memory (a token bucket 68) used by arbiter 66 stores the tokens for a channel until used by the channel. Once a token is used, it is deleted from the token bucket 68. Thus, a single grant request can use up multiple tokens for transmitting multiple packets. The capacity of the token bucket 68 is programmable up to a maximum of 16, in one embodiment. Tokens issued by counter 62 after the token bucket 68 is full are discarded. Varying the capacity of the token bucket 68 as needed is another way to allocate bandwidth to each channel by selecting a maximum bus 52 access time for a channel.

Detailed Description Text (26):
The above-described bandwidth allocation may be performed dynamically as needed by the various channels. Thus, the use of these tokens and counters 62 sets a maximum bandwidth per channel, and its advantages are utilized when there is not enough total bandwidth in the video processor 10 or not enough buffer memory network to accommodate all the channels.

Detailed Description Text (28):
This dynamic bandwidth allocation is particularly useful in the preferred embodiment of the invention, which uses a motherboard for channels 1, 2, and 3 and is expandable to receive two daughter boards, each containing three additional channels. As more channels are added, the likelihood increases that the bandwidth requirements for one or more channels will exceed the bandwidth granted by multiplexer 50 to those channels unless more bandwidth is allocated to those channels.

Detailed Description Text (29):
In the preferred embodiment of the invention, an additional automatic bandwidth allocation circuit is incorporated into multiplexer 50. In this embodiment, threshold detectors are set at various address locations in FIFO buffers 40 for detecting the data level in FIFO buffers 40. For example, a detector may be set at the one-half full location in buffer 40, the three-quarters full location, and the one-packet full location. The detectors may be simple comparators which detect when a certain location in FIFO buffer 40 is addressed for storing a byte from the serial-to-parallel converter 36. In the preferred embodiment, there are both fixed detectors and movable detectors to provide default and customized bandwidth allocation.

Detailed Description Text (30):
If it is detected that the data in a FIFO buffer 40 exceeds a preset threshold, either over a period of time or after a number of occurrences, this signals that the packetizer 44 for that channel needs access to the common bus 52 at a greater rate. In response, a token multiplier 70 for that channel is automatically programmed to multiply the access time for the packetizer 44 for that channel. For example, if the token multiplier 70 for a high bandwidth channel were set to four, then for each access granted to the packetizer 44 (by the simultaneous occurrence of a request and a token) the access time would be multiplied by four to allow four

consecutive packets to be transmitted on bus 52. In one embodiment, the token multiplier can multiply access times two or four times. Since, in the preferred embodiment, a token bucket 68 can hold up to 16 tokens, a maximum bus 52 access time is 16.times.4, or 64 consecutive packets. In other embodiments, the maximum multiplier may be 16 or greater.

Detailed Description Text (32):
Accordingly, bandwidth allocation for each channel is determined automatically, or by a predetermined allocation, or a combination of both.

Detailed Description Text (33):
FIG. 3 is a flowchart illustrating this dynamic bandwidth allocation (or dynamic rate control) for any one of the channels. In step 1, the audio/video signals are stored in FIFO buffer 40.

Detailed Description Text (38):
In step 5, which may occur at any time, the counter 62 for that particular channel is programmed to issue tokens at a predetermined frequency, depending on the channel's bandwidth allocation.

Detailed Description Text (40):
In step 7, once there is both a request for grant and a token issued for that channel, a channel request is granted by the multiplexer 50. The length of time the channel is granted access to bus 52 depends upon the number of tokens in the token bucket 68 and the token multiplier setting for that channel. This token multiplier is determined in step 8 by detecting whether the level in FIFO buffer 40 is above a preset threshold for a period of time (including an instantaneous period). If it is determined in step 8 that the bandwidth allocation must be increased, the token will be effectively multiplied in step 9 so as to provide a longer access time to bus 52. Conversely, the token multiplier may reduce the access time if it is detected that the FIFO buffer 40 level is low.

Detailed Description Text (53):
Due to the various bandwidth capacities of the different communications networks 112 which may be connected to the video processor 10, the maximum bandwidths on the various channels may have to be limited to prevent bandwidth hogging of one or more of the channels, as previously mentioned. In the automatic bandwidth allocation mode, using the token multiplier 70 in FIG. 2, the bandwidth of the network is shared to an optimized extent by the various channels on an as-needed basis. However, if this automatic bandwidth allocation still results in not enough bandwidth to transfer all the video channels' data completely, then the operator of the video processor may intervene by using the external computer 58 (FIG. 1) to limit the upper magnitude of a token multiplier 70 or a token bucket 68 or change the programming of the counters 62 as necessary to optimized the use of the bandwidth of the communication network.

CLAIMS:

1. A video processor having a plurality of channels, each channel for being connected to a source of video data in compressed form, said video processor comprising:

a storage buffer for each of said channels for receiving video data associated with a particular channel;

a packetizer for each channel connected to receive video data from an associated storage buffer;

a bus connected to an output of each packetizer for receiving packets of data output from each packetizer;

an arbiter for receiving grant requests from each of said packetizers to access said bus, each of said packetizers signalling a request for granting access to said bus when it is determined that said storage buffer contains an amount of data greater than a threshold amount;

a dynamic bandwidth allocator for allocating bandwidth on said bus which allows selected channels to have more access to said bus than other channels, said dynamic bandwith allocator issuing tokens to respective channels, said arbiter granting a request from a packetizer to access said bus when there is both at least one token associated with said packetizer and a request for grant by said packetizer; and

a token multiplier for each channel which multiplies a number of tokens accumulated for each channel to increase access time to said bus.

5. The processor of claim 1 wherein said dynamic bandwith allocator allocates bandwidth to each of said channels depending upon the bandwidth requirement for each of said channels.

8. The processor of claim 6 further comprising a token bucket memory for identifying an accumulated number of tokens issued by said token counter for each channel, a token being deleted from said token bucket memory when utilized by said packetizer.

9. The processor of claim 8 wherein said token bucket memory limits a number of accumulated tokens for a respective channel to a selected number of tokens to limit a number of sequential packets which may be transmitted to said bus.

10. The processor of claim 9 wherein a maximum number of tokens stored in each token bucket memory is programmable in order to selectively allocate bandwidth to each channel.

13. A video processor having a plurality of channels, each channel for being connected to a source of video data in compressed form, said video processor comprising:

a storage buffer for each of said channels for receiving video data associated with a particular channel;

a packetizer for each channel connected to receive video data from an associated storage buffer;

a bus connected to an output of each packetizer for receiving packets of data output from each packetizer;

an arbiter for receiving grant requests from each of said packetizers to access said bus, each of said packetizers signalling a request for granting access to said bus when it is determined that said storage buffer contains an amount of data greater than a threshold amount;

a dynamic bandwidth allocator for allocating bandwidth on said bus which allows selected channels to have more access to said bus than other channels, said dynamic bandwith allocator issuing tokens to respective channels, said arbiter granting a request from a packetizer to access said bus when there is both at least one token associated with said packetizer and a request for grant by said packetizer; and

at least one detector detecting an amount of data within said storage buffer for each channel, an amount of data in said storage buffer exceeding a certain amount causing more tokens to be available for a particular channel to allow said packetizer to increase access to said bus,

wherein said at least one detector includes a detector sensing an amount of data needed to fill a complete packet as well as an additional detector detecting an amount of additional data.

15. A video processor having a plurality of channels, each channel for being connected to a source of video data in compressed form, said video processor comprising:

a storage buffer for each of said channels for receiving video data associated with a particular channel;

a packetizer for each channel connected to receive video data from an associated storage buffer;

a bus connected to an output of each packetizer for receiving packets of data output from each packetizer;

an arbiter for receiving grant requests from each of said packetizers to access said bus, each of said packetizers signalling a request for granting access to said bus when it is determined that said storage buffer contains an amount of data greater than a threshold amount;

a dynamic bandwidth allocator for allocating bandwidth on said bus which allows selected channels to have more access to said bus than other channels, said dynamic bandwith allocator issuing tokens to respective channels, said arbiter granting a request from a packetizer to access said bus when there is both at least one token associated with said packetizer and a request for grant by said packetizer; and

a multiplexer board which receives additional boards containing circuitry for one or more channels, the number of channels being processed by said processor being determined by the number of additional boards plugged into said multiplexer board.

18. A video processor having a plurality of channels, each channel for being connected to a video source, said video processor comprising:

a storage buffer for each of said channels for receiving video data associated with a particular channel;

a packetizer for each channel connected to receive video data from an associated storage buffer;

a bus connected to an output of each packetizer for receiving packets of data output from each packetizer;

an arbiter for receiving grant requests from each of said packetizers to access said bus, each of said packetizers signalling a request for granting access to said bus when it is determined that said storage buffer contains an amount of data greater than a threshold amount;

a dynamic bandwidth allocator for allocating bandwidth on said bus which allows selected channels to have more access to said bus than other channels, wherein said dynamic bandwidth allocator comprises a token counter for each of said channels, each of said token counters having a modulus, each of said token counters when cycling through a predetermined state causing a token to be issued for its associated channel, said modulus being determined for each token counter based upon an allocated bandwidth for an associated channel; and

a token multiplier for each channel which multiplies a number of tokens accumulated for each channel to increase access time to said bus.

20. A video processor having a plurality of channels, each channel for being connected to a video source, said video processor comprising:

a storage buffer for each of said channels for receiving video data associated with a particular channel;

a packetizer for each channel connected to receive video data from an associated storage buffer;

a bus connected to an output of each packetizer for receiving packets of data output from each packetizer;

an arbiter for receiving grant requests from each of said packetizers to access said bus, each of said packetizers signalling a request for granting access to said bus when it is determined that said storage buffer contains an amount of data greater than a threshold amount;

a dynamic bandwidth allocator for allocating bandwidth on said bus which allows selected channels to have more access to said bus than other channels, wherein said dynamic bandwidth allocator comprises a token counter for each of said channels, each of said token counters having a modulus, each of said token counters when cycling through a predetermined state causing a token to be issued for its associated channel, said modulus being determined for each token counter based upon an allocated bandwidth for an associated channel; and

least one detector detecting an amount of data within said storage buffer for each channel, an amount of data in said storage buffer exceeding a certain amount causing more tokens to be available for a particular channel to allow said packetizer to increase access to said bus, wherein said at least one detector includes a detector sensing an amount of data needed to fill a complete packet as well as an additional detector detecting an amount of additional data.

22. A video processor having a plurality of channels, each channel for being connected to a video source, said video processor comprising:

a storage buffer for each of said channels for receiving video data associated with a particular channel;

a packetizer for each channel connected to receive video data from an associated storage buffer;

a bus connected to an output of each packetizer for receiving packets of data output from each packetizer;

an arbiter for receiving grant requests from each of said packetizers to access said bus, each of said packetizers signalling a request for granting access to said bus when it is determined that said storage buffer contains an amount of data greater than a threshold amount;

a dynamic bandwidth allocator for allocating bandwidth on said bus which allows selected channels to have more access to said bus than other channels; and

a multiplexer board which receives additional boards containing circuitry for one or more channels, the number of channels being processed by said processor being determined by the number of additional boards plugged into said multiplexer board.